Remarks

Reconsideration and allowance of the subject patent application are respectfully requested.

Applicants acknowledge with appreciation the indication that claims 13, 15, 24, 26, 36, 38, 41, 42 and 52 contain allowable subject matter.

Claim 16 has been amended to more clearly refer to "read request queues" and claim 53 has been amended to correct an obvious misnumbering error. These amendments are not made made for reasons relating to patentability.

The office action contains various references to "Novak-van Hook". See, e.g., 6/2/2005 Office Action, page 2, line 3. In responding to this office action, Applicants have interpreted these references to be references to "Novak-Harriman".

Claims 1-7, 16-18, 27-30, 39, 43-46 and 53 were rejected under 35 U.S.C. Section 103(a) as allegedly being "obvious" over Novak et al. (U.S. Patent No. 6,295,586) in view of Harriman et al. (U.S. Patent No. 6,092,158). Applicants respectfully traverse this rejection.

Novak et al. discloses a memory controller in which a request decoder 310 receives memory requests from memory requestors 210. Novak et al. describes the memory requestors as including the CPU 30, AGP 40 and I/O devices connected to the PCI bus 10. The requests are decoded by the decoder 310 into "primitive" memory operations (i.e., activate, pre-charge, read/write) which are then stored in respective opertion queues AQ (activate operation queue) 340, PQ (pre-charge operation queue) 350 and RWQ (read/write operation queue) 360. Each operation queue 340, 350, 360 operates independently to try and issue its queued operation onto the memory bus 100 in order to initiate the memory request. An SDRAM priority multiplexor (SPM) 270 selects an operation to be sent to the memory 70. Once a memory request is initiated, a read/write control queue (RWCQ) 365 is responsible for tracking the outstanding read or write operations that have been sent to the memory 70. The RWCQ 365 is also connected to the operation queues and provides necessary information about historical operations so that the operation queues can determine when timing and ordering dependencies are met in relation to past operations.

With respect to claim 1, Novak et al. does not disclose a plurality of buffer memories, a multiple resource buffer memory, or a control circuit as claimed. For example, the office action identifies queues 350 and 360 as the "plurality of buffer memories" In Novak et al., the requests from all requestors are supplied to the decoder 310 which then decodes that request into primitive operations (activate, pre-charge, read/write) and supplies these primitive operations to the appropriate queues. As such, queues 350 and 360 are not each operatively coupled to one of a plurality of resources as specified in claim 1.

Novak et al. likewise does not disclose a multiple resource buffer memory for storing requests for main memory access from each of the plurality of resources. The office action identifies RWCQ 365 as the claimed "multiple resource buffer memory." RWCQ 365 stores control signals for use, for example, in the future when data starts to return from the memory. Novak et al. clearly describes that memory requests are initiated when the operation queues issue operations into the memory bus 100 (Novak et al., col. 9, lines 2-5) and there is no description of RWCQ storing or issuing such requests. Because RWCQ 365 is not disclosed as storing requests for memory access, RWCQ 365 cannot constitute the multiple resource buffer memory of claim 1.

Finally, as acknowledged in the office action, Novak et al. does not disclose a control circuit as in claim 1 that controls the transfer of information from the buffer memories to the multiple resource buffer memory and that is operable to control this transfer to reduce the frequency of switching from main memory write operations to main memory read operations.

To cure the acknowledged deficiency, the office action relies on Harriman et al. which is cited for its reference to the grouping of reads and writes in order to "reduce turnaround." Harriman et al., col. 1, lines 43-47.

First, Applicants respectfully submit that Harriman et al. does not remedy the deficiencies of Novak et al. discussed above with respect to, for example, the buffer memories. As such, even if Harriman et al. were forcibly combined with Novak et al., the subject matter of claim 1 would not have resulted.

Second, it is not clear how reads and writes could be grouped between queues 350, 360 and RWCQ 365 of Novak et al. as proposed in the office action to achieve the stated object of reduced turnaround. As discussed above, decoder 310 of Novak et al. receives requests and

decodes the requests into primitive operations which are supplied to appropriate operation queues 340, 350, 360.

> When a read operation is dispatched to the memory 70 by the SPM 370, the control logic 465 loads the VRd 450 with control signals for use in the future when data starts to return. When a write operation is dispatched to the memory 70 by the SPM 370, the control logic 465 loads the VWr 455 with control signals for use in the future when the memory is ready to receive the data to be written. Novak et al., col. 9, lines 43-49.

Because the control logic 465 of Novak et al. loads the RWCQ 365 with control signals based on the dispatching of an operation, this control logic would not be able to perform grouping of reads and writes as proposed in the office action. In other words, one cannot group operations that have already been dispatched. As such, even assuming for the sake of argument that Harriman et al. were suggestive of grouping reads and writes, this grouping would not be effected by a control circuit that controls a transfer of information between what the office action identifies as the buffer memories (i.e., operation queues 350, 360) and what the office action identifies as the multiple resource buffer memory (i.e., RWCQ 365). Consequently, Applicants respectfully submit that the proposed combination of Novak et al. and Harriman et al. would not have resulted in the memory controller of claim 1.

For at least these reasons, Applicants respectfully submit that the subject matter of claim 1 and its dependent claims 2-7 is not made obvious by the proposed combination of Novak et al. and Harriman et al.

In addition, claims 2-7 contain additional patentable features not disclosed in the applied documents.

By way of example, not limitation, in connection with claim 2, the office action references queues 350 and RWQ 360 as showing that the plurality of buffer memories are main memory write queues. However, queue 350 is a pre-charge queue and queue 360 at best could be viewed as one write queue. There is no disclosure of a plurality of buffer memories being main memory write queues.

By way of further example, with regard to claim 4, because write requests are not coupled from the operation queues to RWCQ 365, Novak et al. cannot provide a control circuit that is operable to control the rate at which such requests are coupled.

With respect to claim 16, Novak et al. does not include a main processor related interface, a first resource related interface or a second resource related interface as called for therein. Specifically, the main processor related interface of claim 16 includes a main processor read request queue and a main processor write request queue; the first resource related interface includes at least one of a first resource read request queue and a first resource write request queue; and the second resource related interface includes at least one of a second resource read request queue and a second resource write request queue.

As described above, Novak et al. discloses operation queues 340, 350, 360 which respectively store activate, pre-charge, and read/write operations from all requestors. Consequently, these queues do not constitute a main processor related interface with queue(s) for main processor reads or writes or a first resource related interface with queue(s) for first resource reads or writes or a second resource related interface with queue(s) for second resource reads or writes. Harriman et al. likewise fails to disclose interfaces with such queues and thus the proposed combination of these documents is likewise deficient in this regard with respect to claim 16 and its dependent claims 17 and 18.

In addition, claims 17 and 18 contain additional patentable features not disclosed in the applied documents.

With respect to claim 27, Novak et al. does not disclose storing requests for main memory access from a first resource in a first resource request queue and from a second resource in a second resource request queue. As noted above, Novak et al. does not provide queues that are arranged on the basis of requests from particular resources. Instead, queues 340, 350, 360 contain operations that originate from all resources. Harriman et al. likewise fails to disclose first and second resource queues as claimed and thus the proposed combination of Novak et al. and Harriman et al. is likewise deficient in this regard with respect to claim 27 and its dependent claims 28-30 and 39.

Applicants note that claim 40 has not been rejected based on the proposed combination of Novak et al. and Harriman et al. As such, the rejection of claims 43-46 and 53 (which depend from claim 40) based on this proposed combination is believed to be improper.

Claims 8-12, 19-23, 31-35 and 47-51 were rejected under 35 U.S.C. Section 103(a) as allegedly being "obvious" over the proposed Novak et al-Harriman et al., in view of Jeddeloh et al. (U.S. Patent No. 6,330,647). Applicants respectfully traverse this rejection.

Jeddeloh et al. was applied in connection with its disclosure of an arbiter 210. However, even assuming that such an arbiter were somehow added to the Novak et al.-Harriman et al. combination, Jeddeloh et al. does not remedy the deficiencies of Novak et al. and Harriman et al. with respect to claims 1, 16 and 27, from which claims 8-12, 19-23 and 31-35 depend.

Claims 47-51 depend from claim 40, which has not been rejected based on the combination of Novak et al. and Harriman et al. As such, the rejection of these claims based on this combination in further view of Jeddeloh et al. is improper.

Claims 14, 25, 37 and 40 were rejected under 35 U.S.C. Section 103(a) as allegedly being "obvious" over the proposed Novak et al.-Harriman et al. combination, in further view of Mote, Jr. (U.S. Patent No. 5,666,494). The office action notes that the Novak et al.-Harriman et al. combination does not disclose a resource that is writing to main memory generating a flush signal for initiating the flushing of that resource's write request queue. As noted in the office action, Mote, Jr. makes reference to flushing a posted write buffer to write data to DRAMs 135. However, there is no disclosure or suggestion that the flush signal is generated by the resource that is generating the write requests as specified in these claims. For at least this reason, Applicants respectfully submit that the proposed combination of Novak et al.-Harriman et al. and Mote, Jr. would not have made the subject matter of these claims obvious.

Claim 54 has been added. The subject matter of this claim is fully supported by the original disclosure and no new matter has been added.

Claim 54 is directed to a memory controller comprising a plurality of buffer memories, two or more of the buffer memories being operatively coupled to a different respective one of a plurality of resources requesting access to a main memory and storing information indicative of a request for main memory access from that one of the plurality of resources. A multiple resource buffer memory is coupled to the plurality of buffer memories. A control circuit controls the transfer of requests from the plurality of buffer memories to the multiple resource buffer memory, wherein the control circuit is operable to control the transfer of the requests from the plurality of buffer memories to the multiple resource buffer memory to reduce the frequency of switching from main memory write operations to main memory read operations. Applicants respectfully submit that the applied documents do not disclose and are not suggestive of a memory controller including buffer memories, a multiple resource buffer memory and a control circuit arranged as described in claim 54.

FOULADI et al.
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The pending claims are believed to be in condition for allowance and favorable office action is respectfully requested.

Respectfully submitted,

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